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REMARKS

Claims 4, 11,15 and 24 have been amended to address the informalities noted by the Examiner.

The Examiner rejected a number of claims 1 – 4, 12 – 15 and 23 - 25 under 35 U.S.C. 102(b) as being unpatentable over by U.S. Patent 6,392,712 issued to Gryskiewicz that describes a system for synchronizing interlaced and progressive video signals in view of U.S. Patent 6,915,528. In the Examiner's "Response to Arguments" on page 2 of the Final Office Action mailed June 8, 2006, the Examiner states "It is noted that the receiver in Gryskiewicz automatically formats a video signal for an analog display device with a frame rate of 30 Hz (col. 5, line 63 – col 6, line 5). These are display characteristics." After careful consideration of the section cited by the Examiner, the Applicants respectfully disagree with the Examiner's stated interpretation. The cited section of Gryskiewicz is reproduced below as is the relevant Fig. 1:

"The formerly interlaced data stream 120 may be synchronized with the progressive video data stream 130. In one embodiment of the invention, the progressive stream 130 is received by the transmitter 114 at a 60 Hz frame rate. The interlaced stream 120 is received by the transmitter 106, in the form of alternating odd fields 124a and even fields 124b, at 60 fields per second, for a 30 Hz frame rate. However, the transmitter 106 constructs a new frame 128 each time period and thus transmits at a 60 Hz frame rate, to keep up with the frame rate of the transmitter 114."

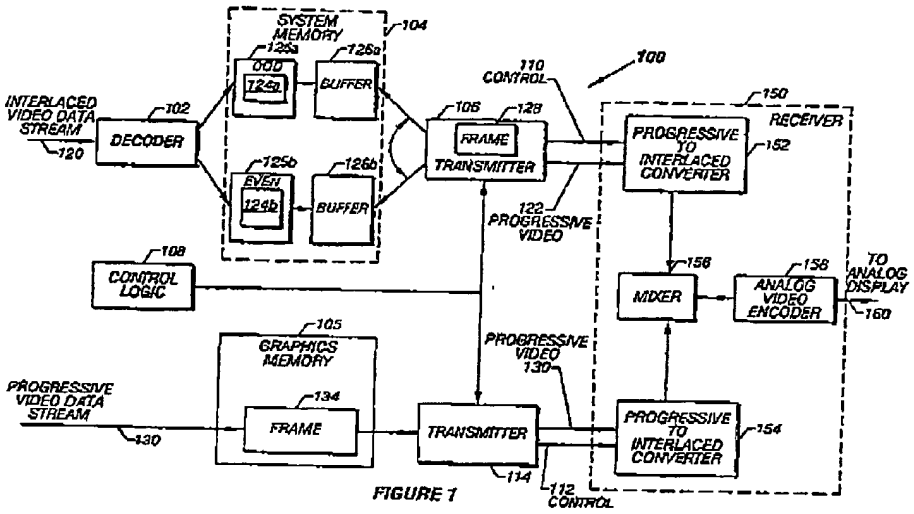


FIGURE 1

Since the progressive stream 130 is received at 60 Hz frame rate and the interlaced stream 120 is received at 60 fields per second (in the form of alternating odd fields 124a and even fields 124b) equal to a 30 Hz frame rate, in order to synchronize the progressive stream 130 and the interlaced stream 120, an additional frame is added to the interlaced stream 120 (thereby assuring both streams 120 and 130 are at the same frame rate of 60 Hz). The procedure described by the Examiner is used by the transmitter 106 "to keep up with the frame rate of the transmitter 114" and has nothing whatsoever to do with the analog display in general.

Furthermore, it appears that in all of the described embodiments of Gryskiewicz, the receiver 150 is ***dedicated*** to a particular analog display and cannot by its very nature be configured in real time as is the inventive configurable real time video processor. Referring to Fig. 1, for example, the receiver 150 is only discussed in only in terms of the type of display to which it is dedicated. For example, if the display is an analog, interlaced display, then the receiver converts the incoming progressive video signals 122 and 130 to interlaced signals by way of the progressive to interlaced converters 152 and 154, respectively. At no point does

Gryskiewicz suggest that the receiver 150 be configured in real time to process signals for any display other than an analog interlaced type display (such as a progressive scan analog device, for example). Therefore, once configured, the receiver 150 can only be used to process video signals for the type of display for which it was originally configured, and no other.

In contrast, the invention describes a configurable real time video processor that can be connected to any display device of any type at any time and based upon the particular display characteristics, the video processor is configured in real time to properly process any incoming signal. At paragraph [0018] of the application:

"the inventive circuit 200 can be used to process video signals for any of a number of different type displays each arranged to display video signals of a corresponding format. In these cases then the video processing circuit 200 is a configurable video processing circuit."

Therefore, the Applicants believe that the rejected claims are not anticipated by the cited reference and respectfully request that the Examiner withdraw the 35 U.S.C. 102(b) rejection thereof.

A number of claims were rejected under 35 U.S.C. 103(a) as being unpatentable over Gryskiewicz in view of number of secondary references that includes: U.S. Publication 2004/0012577), U.S. Patent 6,915,528 issued to McKenna, Official Notice of graphics processors on integrated circuits, and U.S. Publication 2003/006752 of Leyvi. None of these secondary references cure the underlying deficiency of Gryskiewicz of describing a circuit dedicated to a particular display. It appears that the Examiner is using hindsight reconstruction of Gryskiewicz and any of the secondary references with the applicant's own disclosure as a blueprint to recreate the invention from indirect teachings and links in Gryskiewicz and any of the secondary references. For example, the Examiner states on page 8 second paragraph:

"It is logical to then assume that if a signal in progressive format compatible with a display is passed to the invention of Leyvi, conversion will be bypassed. The motivation for this is the same as for any removal of any unnecessary graphics component: to save processing time and power. It would have been obvious to one skilled in the art to modify Gryskiewicz to bypass the unnecessary converter in order to save processing time and power as taught by Leyvi."

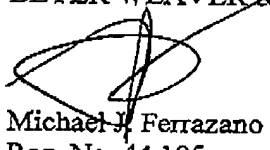
Without using hindsight reconstruction, there is simply no way that one skilled in the art could come up with the claimed invention from the information in Gryskiewicz and Leyvi. All embodiments shown or described in Gryskiewicz include the receiver 150 with dedicated progressive to interlaced converters 152 and 154, while the cited embodiments in Leyvi includes a scan converter that "when the ***target digital video display*** is a DVI compliant display monitor, the scan converter 150 receives EDID from the target digital video display" at paragraph [0025]. Therefore Leyvi relies upon the display being a ***digital display*** in order to provide the relied upon scan conversion whereas Gryskiewicz is strictly limited to ***analog displays*** and therefore neither reference cures the fundamental deficiencies of the other. For at least these reasons, the Applicant believes that the claims rejected under 35 U.S.C. 103(a) and Official Notice is unsupported by the art and respectfully request that the rejection be withdrawn.

CONCLUSION

The Applicants believe that claims 1 – 33 are allowable in view of the remarks above. Should the Examiner believe that a further telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,

BEYER WEAVER & THOMAS, LLP



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